

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	John Snyder	Examiner: L. Pham
Application No.:	09/928,124	
Filing Date:	August 10, 2001	
Title:	A FABRICATION METHOD FOR A DEVICE FOR REGULATING FLOW OF ELECTRIC CURRENT WITH HIGH DIELECTRIC CONSTANT GATE INSULATING LAYER AND SOURCE/DRAIN FORMING SCHOTTKY CONTACT OR SCHOTTKY-LIKE REGION WITH SUBSTRATE	Group Art Unit: 2814

Stamp: OIPE JC66 JUN 26 2003 PATENT & TRADEMARK OFFICE

TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this document is being sent via First Class U.S. mail addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 23 day of June, 2003.

KrisAnne Popovits
KrisAnne Popovits

Dear Sir:

The following documents are enclosed in connection with the above-referenced patent application:

1. Information Disclosure Statement Under 37 CFR 1.97(c) (2 pages);
2. Form PTO/SB/08A (6 pages, submitted in duplicate);
3. Copies of 65 References Cited;
4. Fee Determination (After Amendment of Claims) (1 page);
5. Check No. 956872 in the amount of \$180; and
6. Return Receipt Postcard.

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JUN 30 2003

TECHNOLOGY CENTER 2800

Date: 6.23.03

Respectfully submitted,

DORSEY & WHITNEY LLP
Customer Number 25763

By: *Jason R. Kraus*
Jason R. Kraus (Reg. No. 42,765)
Intellectual Property Department
Suite 1500, 50 South Sixth Street
Minneapolis, MN 55402-1498
(612) 340-5617

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FEE DETERMINATION (After Amendment of Claims)

Complete if Known

Application No.	09/928,124
Filing Date	August 10, 2001
First Named Inventor	John Snyder
Group Art Unit	2814
Examiner Name	L. Pham
Atty. Docket Number	14466

Claims as Amended in Response to Office Action dated: N/A

METHOD OF PAYMENT (Check One)		AMENDMENT FEE CALCULATION (Continued)																																																																	
<p>1. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge indicated fees and credit any over payments to: Deposit Account No.: 04-1420 Deposit Account Name: DORSEY & WHITNEY LLP</p> <p><input checked="" type="checkbox"/> Charge any additional fee required under 37 C.F.R. 1.16 and 1.17</p> <p><input checked="" type="checkbox"/> Applicant claims small entity status (see 37 C.F.R. 1.27)</p> <p>2. <input checked="" type="checkbox"/> Check Enclosed</p>		<h3>3. ADDITIONAL FEES</h3> <table><thead><tr><th>Large Entity Fee</th><th>Small Entity Fee</th><th>Fee Description</th><th>Fee Paid</th></tr></thead><tbody><tr><td>110</td><td>55</td><td>Extension for reply within first month</td><td></td></tr><tr><td>410</td><td>205</td><td>Extension for reply within second month</td><td></td></tr><tr><td>930</td><td>465</td><td>Extension for reply within third month</td><td></td></tr><tr><td>1,450</td><td>725</td><td>Extension for reply within fourth month</td><td></td></tr><tr><td>1,970</td><td>985</td><td>Extension for reply within fifth month</td><td></td></tr><tr><td>1,300</td><td>650</td><td>Issue Fee-Utility/Reissue</td><td></td></tr><tr><td>320</td><td>160</td><td>Notice of Appeal</td><td></td></tr><tr><td>320</td><td>160</td><td>Filing brief in support of appeal</td><td></td></tr><tr><td>280</td><td>140</td><td>Request for oral hearing</td><td></td></tr><tr><td>110</td><td>55</td><td>Terminal Disclaimer Fee</td><td></td></tr><tr><td>110</td><td>55</td><td>Petition to revive – unavoidable</td><td></td></tr><tr><td>1,300</td><td>650</td><td>Petition to revive – unintentional</td><td></td></tr><tr><td>130</td><td>130</td><td>Petitions to the Commissioner</td><td></td></tr><tr><td>180</td><td>180</td><td>Submission of IDS</td><td>\$180.00</td></tr><tr><td>750</td><td>375</td><td>Request for Continued Examination (RCE)</td><td></td></tr></tbody></table> <p>Other fee (specify):</p> <p>Subtotal (2) \$180.00</p> <p>Total Amount of Payment: \$180.00</p>		Large Entity Fee	Small Entity Fee	Fee Description	Fee Paid	110	55	Extension for reply within first month		410	205	Extension for reply within second month		930	465	Extension for reply within third month		1,450	725	Extension for reply within fourth month		1,970	985	Extension for reply within fifth month		1,300	650	Issue Fee-Utility/Reissue		320	160	Notice of Appeal		320	160	Filing brief in support of appeal		280	140	Request for oral hearing		110	55	Terminal Disclaimer Fee		110	55	Petition to revive – unavoidable		1,300	650	Petition to revive – unintentional		130	130	Petitions to the Commissioner		180	180	Submission of IDS	\$180.00	750	375	Request for Continued Examination (RCE)	
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<h3>AMENDMENT FEE CALCULATION</h3> <h4>1. EXTRA* CLAIM FEES</h4> <table><thead><tr><th>Claims Remaining after Amendment</th><th>Highest Number Previously Paid for</th><th>Present Extra</th><th>Fee from Below*</th><th>Additional Fee</th></tr></thead><tbody><tr><td>Total</td><td>-</td><td>=</td><td>x</td><td>=</td></tr><tr><td>Indep.</td><td>-</td><td>=</td><td>x</td><td>=</td></tr><tr><td>First Presentation of Multiple Dependent Claim</td><td></td><td></td><td>x</td><td>=</td></tr><tr><td colspan="5">Subtotal (1)</td></tr></tbody></table> <p>*Calculation of Extra Claim Fees</p> <table><thead><tr><th>Large Entity Fee</th><th>Small Entity Fee</th><th>Fee Description</th></tr></thead><tbody><tr><td>18</td><td>9</td><td>Claims in excess of 20</td></tr><tr><td>84</td><td>42</td><td>Independent claims in excess of 3</td></tr><tr><td>280</td><td>140</td><td>Multiple dependent Claim</td></tr><tr><td>84</td><td>42</td><td>Reissue independent claims over original patent</td></tr><tr><td></td><td></td><td>Reissue claims in excess of 20 and over original patent</td></tr></tbody></table>		Claims Remaining after Amendment	Highest Number Previously Paid for	Present Extra	Fee from Below*	Additional Fee	Total	-	=	x	=	Indep.	-	=	x	=	First Presentation of Multiple Dependent Claim			x	=	Subtotal (1)					Large Entity Fee	Small Entity Fee	Fee Description	18	9	Claims in excess of 20	84	42	Independent claims in excess of 3	280	140	Multiple dependent Claim	84	42	Reissue independent claims over original patent			Reissue claims in excess of 20 and over original patent																							
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Submitted by:

CUSTOMER NUMBER

25763

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Intellectual Property Department
50 South Sixth Street, Suite 1500
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Name: Jason R. Kraus

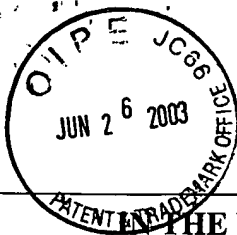
Reg. No.: 42,765

Telephone: (612) 340-5617

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Signature:

Date: 6-23-03



Docket: 14466

THE UNITED STATES PATENT AND TRADEMARK OFFICE	
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Examiner:	L. Pham
Group Art Unit:	2814

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97(c)**

Commissioner for Patents
P. O. Box 1450
Alexandria, Virginia 22313-1450

I hereby certify that this document is being sent via First Class U.S. mail
addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-
1450 on this 23 day of June, 2003


KrisAnne Popovits

Dear Sir:

Pursuant to 37 CFR § 1.97(c), the references listed on the attached Form PTO/SB/08A (7 sheets, submitted in duplicate) are brought to the attention of the Examiner for consideration in connection with the examination of the above-identified patent application. Copies of the identified references are enclosed as necessary. This Information Disclosure Statement ("IDS") is filed on or before the mailing date of a final office action or a notice of allowance is accompanied by the fee set forth in 37 CFR § 1.17(p).

Payment of Fee Under 37 CFR § 1.17(p)

The fee under 37 CFR § 1.17(p), required for submission of an IDS under 37 CFR § 1.97(c), is enclosed, as referenced in the attached Fee Transmittal Sheet.

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06/27/2003 WAREDELRI 00000004 09928124
01 FC:1806 180.00 DP

Pursuant to the Manual of Patent Examining Procedure, Chapter 609, Applicant requests that the Examiner consider each of the listed documents and initial and return to the undersigned a copy of the enclosed PTO/SB/08A (submitted in duplicate).

Respectfully submitted,

DORSEY & WHITNEY LLP
Customer Number 25763

Date: 6.23.03

By: 

Jason R. Kraus
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Intellectual Property Department
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JUN 30 2003

TECHNOLOGY CENTER 2800

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Application Number 09/928,124

Filing Date August 10, 2001

First Named Inventor John Snyder

Art Unit 2814

Examiner Name L. Pham

Sheet 1 of 6 Attorney Docket Number 14466

U.S. PATENT DOCUMENTS

*Examiner Initials	Cite No.	DOCUMENT NUMBER Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 4,053,924	10-11-1977	Roman et al.	
		US- 4,300,152	11-10-1981	Lepselter	
		US- 4,942,441	7-17-1990	Konishi et al.	
		US- 5,040,034	8-13-1991	Murakami et al.	
		US- 5,079,182	1-7-1992	Ilderem et al.	
		US- 5,323,053	6-21-1994	Luryi et al.	
		US- 5,361,225	11-1-1994	Ozawa	
		US- 5,444,302	8-22-1995	Nakajima et al.	
		US- 5,663,584	9-2-1997	Welch	
		US- 5,760,449	6-2-1998	Welch	
		US- 5,767,557	6-16-1998	Kizilyalli	
		US- 5,801,398	9-1-1998	Hebiguchi	

FOREIGN PATENT DOCUMENTS

*Examiner Initial	Cite No.	FOREIGN PATENT DOCUMENT		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	TRANSLATION	
		Country Code:	Number - Kind Code (if known)				YES	NO
		EP	0 603 102 A2	6-22-1994			<input checked="" type="checkbox"/>	<input type="checkbox"/>
		PCT	WO 01/45157 A1	6-21-2001			<input type="checkbox"/>	<input type="checkbox"/>
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EXAMINER SIGNATURE

DATE CONSIDERED

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Application Number 09/928,124

Filing Date August 10, 2001

First Named Inventor John Snyder

Art Unit 2814

Examiner Name L. Pham

Sheet

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of

6

Attorney Docket Number 14466

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		US- 5,883,010	3-16-1999	Merrill et al.	
		US- 6,037,605	3-14-2000	Yoshimura	
		US- 6,160,282	12-12-2000	Merrill	
		US- 6,268,636	7-31-2001	Welch	
		US- 6,323,528	11-27-2001	Yamazaki et al.	
		US- 6,353,251	3-5-2002	Kimura	
		US- 6,420,742	7-16-2002	Ahn et al.	
		US- 6,509,609	1-21-2003	Zhang et al.	
		US- 2001/0024847 A1	9-27-2001	Snyder	
		US- 2002/0030231	3-14-2002	Okawa et al.	
		US-			

FOREIGN PATENT DOCUMENTS

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		Country Code:	Number - Kind Code (if known)				YES	NO
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(use as many sheets as necessary)

Application Number	09/928,124
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First Named Inventor	John Snyder
Art Unit	2814
Examiner Name	L. Pham
Attorney Docket Number	14466

Sheet 3 of 6

OTHER DOCUMENTS - NON-PATENT LITERATURE DOCUMENTS

*Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	TRANSLATION	
			YES	NO
		LEPSELTER, M.P., SZE, S.M. <u>SB-IGFET: An Insulated Gate Field Effect Transistor Using Schottky Barrier Contacts for Source and Drain.</u> Proceedings of the IEEE, August 1968; pp. 1400-1402.	<input type="checkbox"/>	<input type="checkbox"/>
		LEPSELTER, M.P., MACRAE, A.U., MACDONALD, R.W. <u>SB-IGFET, II: An Ion Implanted IGFET Using Schottky Barriers.</u> Proceedings of the IEEE, May 1969; pp. 812-813.	<input type="checkbox"/>	<input type="checkbox"/>
		KISAKI, Hitoshi. <u>Tunnel Transistor.</u> Proceedings of the IEEE, July 1973; pp. 1053-1054.	<input type="checkbox"/>	<input type="checkbox"/>
		KOENEKE, C.J., SZE, S.M., LEVIN, R.M., KINSBRON, E. <u>Schottky MOSFET for VLSI.</u> IEDM, 1981; pp. 367-370.	<input type="checkbox"/>	<input type="checkbox"/>
		SUGINO, M., AKERS, L.A., REBESCHINI, M.E. <u>CMOS Latch-Up Elimination Using Schottky Barrier PMOS.</u> IEDM, 1982; pp. 462-465.	<input type="checkbox"/>	<input type="checkbox"/>
		KOENEKE, C.J., LYNCH, W.T. <u>Lightly Doped Schottky MOSFET.</u> IEDM, 1982; pp. 466-469.	<input type="checkbox"/>	<input type="checkbox"/>
		MOCHIZUKI, T., WISE, K.D. <u>An n-Channel MOSFET with Schottky Source and Drain.</u> IEEE Electron Device Letters, EDL-5, No. 4, April 1984; pp. 108-111.	<input type="checkbox"/>	<input type="checkbox"/>
		OH, C.S., KOH, Y.H., KIM, C.K. <u>A New P-Channel MOSFET Structure with Schottky Clamped Source and Drain.</u> IEDM, 1984; pp. 609-612.	<input type="checkbox"/>	<input type="checkbox"/>
		SWIRHUN, Stanley E., et al. <u>A VLSI Suitable Schottky Barrier CMOS Process.</u> IEEE Transactions on Electron Devices, ED-32, No. 2, February 1985; pp. 194-202.	<input type="checkbox"/>	<input type="checkbox"/>
		TOVE, P.A., BOHLIN, K., MASSZI, F., NORDE, H., NYLANDER, J., TIREN, T., MAGNUSON, U. <u>Complementary Si MESFET Concept Using Silicon-on-Sapphire Technology.</u> IEEE Electron Device Letters, Vol. 9, No. 1, January 1988; pp. 47-49.	<input type="checkbox"/>	<input type="checkbox"/>
		TOVE, P.A., BOHLIN, K.E., NORDE, H., MAGNUSON, U., TIREN, J., SODERBARG, A., ROSLING, M., MASSZI, F., NYANDER, J. <u>Silicon IC Technology Using Complementary MESFETs.</u> Solid State Devices, Elsevier Science Publishers (North Holland), 1988; pp. 607-609.	<input type="checkbox"/>	<input type="checkbox"/>

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Application Number	09/928,124
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Sheet 4 of 6

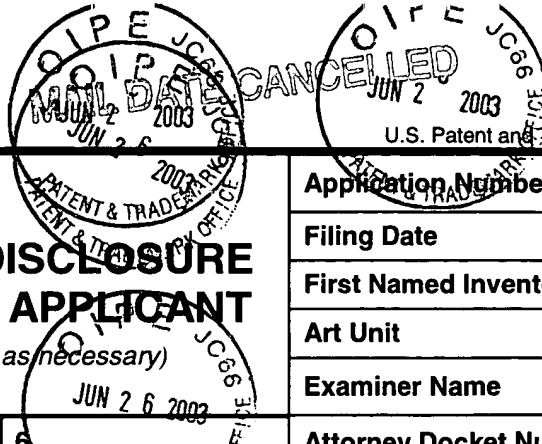
OTHER DOCUMENTS - NON-PATENT LITERATURE DOCUMENTS

*Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	TRANSLATION	
			YES	NO
		TSUI, B., CHEN, M. A Novel Process for High-Performance Schottky Barrier PMOS. <i>J. Electrochem Soc.</i> , Vol. 136, No. 5, May 1989; pp. 1456-1459.	<input type="checkbox"/>	<input type="checkbox"/>
		MISRA, D., SIMHADRI, V.S. A Survey of the Potential of an IrSi Schottky Barrier MOSFET Based on Simulation Studies. <i>Solid State Electronics</i> , Vol. 35, No. 6, 1992; pp. 829-833.	<input type="checkbox"/>	<input type="checkbox"/>
		HATTORI, Reiji, NAKAE, Akihiro, SHIRAFUJI, Junji. A New Type of Tunnel-Effect Transistor Employing Internal Field Emission of Schottky Barrier Junction. <i>Japan J. Appl. Phys.</i> , Vol. 31, 1992; pp. L1467-L1469.	<input type="checkbox"/>	<input type="checkbox"/>
		HATTORI, Reiji, SHIRAFUJI, Junji. Numerical Simulation of Tunnel Effect Transistors. <i>Japan J. Appl. Phys.</i> , Vol. 33, 1994; pp. 612-618.	<input type="checkbox"/>	<input type="checkbox"/>
		TUCKER, J.R., WANG, C., LYDING, J.W., SHEN, T.C., ABELN, G.C. Nanometer Scale MOSFETs and STM Patterning on Si. <i>SSDM 1994</i> , August 1994; pp. 322-324.	<input type="checkbox"/>	<input type="checkbox"/>
		TUCKER, J.R., WANG, C., CARNEY, P.S. Silicon Field-Effect Transistor Based on Quantum Tunneling. <i>Applied Physics Letters</i> , Vol. 65, No. 5, 1 August 1994; pp. 618-620.	<input type="checkbox"/>	<input type="checkbox"/>
		KIMURA, Mitsuteru, MATSUDATE, Tadashi. A New Type of Schottky Tunnel Transistor. <i>IEEE Electron Device Letters</i> , EDL-15, No. 10, October 1994, pp. 412-414.	<input type="checkbox"/>	<input type="checkbox"/>
		SNYDER, John P., HELMS, C.R., NISHI, Yoshio. Experimental Investigation of a PtSi Source and Drain Field Emission Transistor. <i>Applied Physics Letters</i> , Vol. 67, No. 10, 4 September 1995; pp. 1420-1422.	<input type="checkbox"/>	<input type="checkbox"/>
		WOLF, Stanley. Silicon Processing for the VLSI Era. Volume 3: The Submicron MOSFET, Lattice Press, Sunset Beach, CA, 1995; pp. 523-528.	<input type="checkbox"/>	<input type="checkbox"/>
		SHASTON, S.A., ISMAIL, K., CHU, J.O., CHAN, K. A MOS Transistor with Schottky Source/Drain Contacts and a Self-Aligned Low-Resistance T-gate. <i>Microelectronics Engineering</i> , Vol. 35, 1997; pp. 361-363.	<input type="checkbox"/>	<input type="checkbox"/>
		NISHISAKA, Mika, ASANO, Tanemasa. Reduction of the Floating Body Effect in SOI MOSFETs by Using Schottky Source/Drain Contacts. <i>Japan J. Appl. Phys.</i> , Vol. 37, March 1998; pp. 1295-1299.	<input type="checkbox"/>	<input type="checkbox"/>

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Examiner Name	L. Pham
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Sheet

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of

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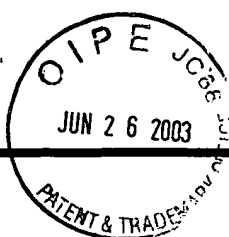
OTHER DOCUMENTS - NON-PATENT LITERATURE DOCUMENTS

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			YES	NO
		WANG, C., SNYDER, John P., TUCKER, J.R. <u>Sub-50nm PtSi Schottky Source/Drain p-MOSFETs</u> . 56 th Annual Device Research Conference Digest, June 1998, pp. 72-73.	<input type="checkbox"/>	<input type="checkbox"/>
		ZHAO, Q.T., KLINKHAMMER, F., DOLLE, M., KAPPIUS, L., MANTL, S. <u>Nanometer Patterning of Epitaxial CoSi₂/Si(100) for Ultrashort Channel Schottky Barrier Metal-Oxide-Semiconductor Field Effect Transistors</u> . Applied Physics Letters, Vol. 74, No. 3, 18 January 1999; pp. 454-456.	<input type="checkbox"/>	<input type="checkbox"/>
		WANG, C., SNYDER, John P., TUCKER, J.R. <u>Sub-40nm PtSi Schottky Source-Drain Metal-Oxide-Semiconductor Field-Effect-Transistors</u> . Applied Physics Letters, Vol. 74, No. 8, 22 February 1999; pp. 1174-1176.	<input type="checkbox"/>	<input type="checkbox"/>
		SNYDER, John P., HOLMS, C.R., NISHI, Yoshio. <u>Analysis of the Potential Distribution in the Channel Region of a Platinum Silicided Source/Drain Metal Oxide Semiconductor Field Effect Transistor</u> . Applied Physics Letters, Vol. 74, No. 22, 31 May 1999; pp. 3407-3409.	<input type="checkbox"/>	<input type="checkbox"/>
		SAITOH, W., YAMAGAMI, S., ITOH, A., ASADA, M. <u>35nm Metal Gate SOI-p-MOSFETs with PtSi Schottky Source/Drain</u> . 57 th Annual Device Research Conference Digest, June 1999; pp. 30-31.	<input type="checkbox"/>	<input type="checkbox"/>
		TUCKER, J.R. <u>Schottky Barrier MOSFETs for Silicon Nano-electronics</u> . IEEE Frontiers in Electronics, January 1997; pp. 97-100.	<input type="checkbox"/>	<input type="checkbox"/>
		LAPLANTE, Philip A. (Editor-in-Chief). <u>Comprehensive Dictionary of Electrical Engineering</u> . IEEE Press, 1999, page 97.	<input type="checkbox"/>	<input type="checkbox"/>
		MULLER, Richard S. and KAMINS, Theodore I. <u>Device Electronics for Integrated Circuit</u> . John Wiley & Sons, Second Edition, 1977, 1986, pp. 448, 505-511.	<input type="checkbox"/>	<input type="checkbox"/>
		PERRET. <u>Modular Series On Solid State Devices, vol. I Semiconductor Fundamentals</u> , Addison-Wesley, 1983; pp. 29-33.	<input type="checkbox"/>	<input type="checkbox"/>
		NEUDECK, Gerold W. <u>Volume II: The PN Junction Diode, Modular Series On Solid State Devices</u> . Addison-Wesley, 1983; pp. 8-10.	<input type="checkbox"/>	<input type="checkbox"/>
		On-line Encyclopedia Britannica, 2001, definition of "rare-earth element.", date not established; 2 pages.	<input type="checkbox"/>	<input type="checkbox"/>

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DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Application Number	09/928,124
Filing Date	August 10, 2001
First Named Inventor	John Snyder
Art Unit	2814
Examiner Name	L. Pham
Attorney Docket Number	14466

Sheet 6 of 6

OTHER DOCUMENTS - NON-PATENT LITERATURE DOCUMENTS

*Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	TRANSLATION	
			YES	NO
		SZE, S.M. <u>Physics of Semiconductor Devices</u> , John Wiley & Sons, Second Edition, 1981; pp. 293-294.	<input type="checkbox"/>	<input type="checkbox"/>
		CALVET, L. E., LUEBBEN, H., REED, M.A., WANG, C., SNYDER, J.P., and TUCKER, J.R. <u>Subthreshold and scaling of PtSi Schottky barrier MOSFETs</u> , 2000 Academic Press, <i>Superlattices and Microstructures</i> , Vol. 28, No. 5/6; pp. 501-506.	<input type="checkbox"/>	<input type="checkbox"/>
		WOLF, Stanley. <u>Silicon Processing for the VLSI Era, Vol. 3: The Submicron MOSFET</u> . Lattice Press, 1995; pp. 183-187.	<input type="checkbox"/>	<input type="checkbox"/>
		Web page "provided by Laurie Calvet", "Device Physics of the SBMOSFET", http://www.eng.yale.edu/reedlab/research/semicond.html , date not established; 7 pages.	<input type="checkbox"/>	<input type="checkbox"/>
		WINSTEAD, B. and RAVAIOLI, U. <u>Simulation of Schottky Barrier MOSFET's with a Coupled Quantum Injection/Monte Carlo Technique</u> . <i>IEEE Transactions on Electron Device</i> , Vol. 47, No. 6, June 2000; pp. 1241-1246.	<input type="checkbox"/>	<input type="checkbox"/>
		GANG, D., XIAOYAN, L., LEI, S., JIAPING, Y., RUQI, H., HOULET, P., and FUJITAN, H. <u>Monte Carlo Simulation of 50nm n-Channel Schottky Barrier Tunneling Transistors</u> . <i>Chinese Journal of Electronics</i> , Vol. 11, No. 2, April 2002; pp. 200-203.	<input type="checkbox"/>	<input type="checkbox"/>
		RISHTON, S.A., ISMAIL, K., CHU, J.O., CHAN, K.K., LEE, K.Y. <u>New Complimentary metal-oxide semiconductor technology with self-aligned Schottky source/drain and low-resistance T gates</u> . <i>J. Vac. Sci. Technol. B</i> , 15(6), Nov/Dec 1997, pp. 2795-2798.	<input type="checkbox"/>	<input type="checkbox"/>
		KEBZIERSKI, J., XUAN, P., SUBRAMANIAN, V., BOKOR, J., KING, T.-J., HU, C., ANDERSON, E. <u>A 20 nm gate-length ultra-thin body p-MOSFET with silicide source/drain</u> . <i>Superlattices and Microstructures</i> , Vol. 28, No. 5/6, 2000, pp. 445-452.	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>

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